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GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF RESEARCH ADMINISTRATION

RESEARCH PROJECT INITIATION

Date: June 22, 1972

Project Title: **Resident Fellowship Program in Computer Science**

Project No: **E-21-622**

Principal Investigator: **Dr. M. A. Tapia**

Sponsor: **NASA - Langley Research Center; Hampton, Virginia**

Agreement Period: From June 12, 1972 Until September 11, 1973

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RA-3 (6-71)

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RESEARCH PROJECT TERMINATION

Date: November 27, 1974

Project Title: Resident Fellowship Program in Computer Science

Project No: E-21-622

Principal Investigator: Dr. M. A. Tapia

Sponsor: NASA - Langley Research Center; Hampton, Virginia

Effective Termination Date: 9/12/74

Clearance of Accounting Charges: 9/12/74

Grant Closeout Actions Remaining:

Gov't. Property Inventory & Related Cert.
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Final Fiscal Report

Electrical Engineering

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RA-4 (5-70)

E-21-622

RESIDENT FELLOWSHIP PROGRAM

IN

COMPUTER SCIENCE

SEMI-ANNUAL STATUS REPORT
NASA GRANT NO. NGR 11-002-158

JUNE 12, 1972
TO
DEC. 12, 1972

BY

MOIEZ A. TAPIA

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
LANGLEY RESEARCH CENTER
HAMPTON, VIRGINIA

ATTENTION: MR. RICHARD MORRIS, PRECEPTOR
MR. MILNER H. ESKEW, JR., NASA TECHNICAL OFFICER
MR. DONALD H. CARSON, GRANT ADMINISTRATOR

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RESIDENT FELLOW PROGRAM

IN

COMPUTER SCIENCE

MOIEZ A. TAPIA

I. Abstract

The report describes my assignment in the Analysis and Computation Division of the NASA, Langley Research Center. The goals and purposes of my specific task assignments, technical approaches taken for achieving them, their present state, and plans for the future are also given.

II. General Assignment

The Langley Computer Complex has five large-scale scientific computers operating in a multi-program, highly interactive environment under the control of extremely complex operating systems software which is undergoing nearly continuous modification to provide new or improved services. Effort is underway to develop instrumentation systems for collection of data on processor-peripheral communications and for monitoring of operating system performance.

My principal assignment is in the completion, testing and application of a Statistical Data Collection System. This system employs a large number of high-speed test-probes, integrated-circuit logic and storage media for capturing and collecting desired events. The IC logic is

designed for each specific application to provide the event and time information desired.

III. Specific Task Assignments

(a) Study of Disc Performance: It appears, at the present time, that one of the largest bottlenecks which is limiting the throughput of programs in computers is the disc systems. Mr. Richard Staib developed and designed the Statistical Data Collection System as well as plug-in modules to measure the number of words per record, the data transfer time delay, the head position time, the number of reads and writes per unit time and the number of parity errors. I spent several weeks reviewing his design as well as studying the hardware and software aspects of the computer network at the Center in general, and the disc systems in particular.

On Dec. 1, 1972 and Dec. 4, 1972, Mr. Staib and I connected the Statistical Data Collection System to the disc controller of a CDC-6400 computer. On examining the data collected by the system it appeared that some of the modules measuring disc performance were malfunctioning. He and I plan to check out these modules in a couple of weeks and connect the

SDC system to the disc controller.

The data obtained will help us determine the present state of performance of the disc system and will provide useful information for determining the specifications for a Mass Storage System that is currently being considered to be introduced at the Center.

(b) Study of Magnetic Tape Performance:

In order to determine the requirements for a Mass Storage System, it is necessary to know the various ways the users at the Center are using magnetic tapes, the distribution of lengths of records they write on them and the frequency of reading the tapes.

I designed plug-in modules to read the lengths of records written on magnetic tapes, the number of read and write commands issued per second, and the number of EOF (end of file), rewind, rewind/unload and backspace commands per second. Also, in order to provide interface between these modules and Mr. Staib's Statistical Data Collection System, I designed address line selector and priority selector units. The modules will receive signals from the probes connected to both the units of a CDC 3623 Tape Controller. Each unit has 4 channels coming into it and 8 channels going out to 8 possible tape transport units via 4x8 switches. The controller box includes all the test

points necessary in order to obtain the signals we need to gather the desired data. Data pertaining to parity error, for example, cannot be obtained from transport units. Knowing of occurrence of a parity error is necessary in order to measure the lengths of correctly written and/or read records. The number of the transport unit selected will be obtained by reading the bits 0, 1 and 2 of the function code after "connect" signal has been received. Recording this information will enable us to correlate the data obtained and the data on dayfile. Since the memory unit in the Statistical Data Collection System has 2048 locations, 128 locations can be conveniently assigned per transport unit, making it possible to track the data going to all 16 transport units.

The plug-in modules are designed and remain to be built and checked out. It is anticipated that the modules will be ready for connecting to the tape controller around the end of the first quarter of 1973.

(c) Study of CPU Performance:

I am currently studying a CDC-6600 Central Processor Unit. I plan to design plug-in modules for measuring the activity of various arithmetic units, conflicts in their accesses, the number of instructions (in the stack and the central memory) executed per unit time, etc.

This will give us information regarding the present state of performance of the CPU. If any changes in the hardware and/or software are made, then the effect of these changes on the CPU performance can be determined by monitoring CPU with the Statistical Data Collection System with these modules in it.

The modules are anticipated to be ready for installation around the beginning of the 3rd quarter of 1973.

(d) Study of I/O Channel Performance:

Some time in the 2nd quarter of 1973, I plan to consult with the System Analysts in the Division to determine, if the activity of any of the I/O channels need to be measured. Depending on the results of the consultation, plans for this specific task will be formulated later.

(e) Computer Program Development:

In order to facilitate the design of logic modules, I successfully completed a program for minimizing the number of states in a sequential system.

The work on developing a program for an incompletely specified sequential system is still in progress. It is expected to be completed by the end of the first quarter of 1973.

IV. Other Activities

I had several opportunities to participate in the discussions of computer generated images, the Advanced Scientific Computer of Texas Instruments, air-borne digital computers, Comress computer monitor devices, transducers of Kistler Instruments Co., Computer Corporation Design desk calculators. Also, I had an opportunity to attend the Computer Evaluation User Group Conference held during October 17-20, 1972 in Washington, D.C.

Time permitting, I hope to be involved in a number of computer-related activities such as study of fault tolerant computers, advanced computer architecture, graphic systems for real-time displays and scene generation.

V. Conclusion

My major effort has been and will continue to be in the area of computer performance evaluation. This will provide useful information regarding the present state of performance and indicate the areas which may be considered for tuning to improve the system performance.

I have been receiving a very relevant and invaluable experience in modern engineering practice as well as advanced technologies in the burgeoning area of computers and their various applications.

E-21-622

RESIDENT FELLOWSHIP PROGRAM

IN

COMPUTER SCIENCE

SEMI-ANNUAL STATUS REPORT NO. 2
NASA GRANT NO. NGR 11-002-158

DEC. 12, 1972
TO
OCT. 31, 1973

BY

MOIEZ A. TAPIA

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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HAMPTON, VIRGINIA

ATTENTION:

MR. RICHARD MORRIS, NASA TECHNICAL MONITOR AND PRECEPTOR
MR. WILLIAM F. GIANNINI, GRANT ADMINISTRATOR

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RESIDENT FELLOW PROGRAM

IN

COMPUTER SCIENCE

MOIEZ A. TAPIA

I. Review of Earlier Work

My principal assignment in the Analysis and Computation Division of the Langley Research Center is the evaluation of the performance of various subsystems in the Computer Complex using Statistical Data Collection System. The system uses a large number of high-speed test-probes, integrated-circuit logic and storage media for capturing and collecting desired events.

As reported in the earlier report, some of the first set of modules for monitoring a disc controller had some malfunction in them and hence re-designing the modules using high-speed logic seemed desirable. This was delayed due to unavailability of logic gates required for the design.

I designed plug-in modules for monitoring the tape storage system in order to determine the distribution of lengths of records written and read, the user frequency of reading and writing these tapes, etc., in order to obtain the information necessary for determining the requirements for a Mass Storage System being considered at the Center. By the end of November, 1972, I completed the design for the modules including the drawings for the circuit. The wiring of the logic card had to be postponed due to unavailability of some of the required logic gates.

Also, I studied, in December, 1972, the hardware and software details pertaining to a CDC-6600 Central Processor Unit

II. Status of Specific Task Assignments

(a) Study of Disc Performance:

Richard Staib, Edward Phillips and I redesigned the plug-in modules to be used with the Statistical Data Collection System (SDCS) for monitoring the activities in the disc storage system. We also designed circuits for simulating events that could occur in the disc storage system. It took a few weeks in order to debug all the modules as well as the SDCS. The whole system was hooked onto test-points of the disc controllers Z_0, Z_3 and Z_4. The data was collected on tapes on September 24, 25, 26 and 27, 1973. The data was reduced using a computer program used for the purpose and plots were obtained.

Gathering of additional data was discontinued, since we observed that certain locations in the memory had a bit or two turned to the value of "1" erroneously. Even though more data must be gathered before drawing any definite conclusions, the following observations are very obvious:

(1) The total activity on Z_3, the job disc is very low. The total activity time ("duty cycle") remained below 5% most of the time and reached a peak of 10%, indicating a very inefficient utilization of disc.

(2) The total activity time reached a peak of 60% and 80% in the case of discs Z_4 and Z_0, respectively.

(3) Most of the records in Z_0 and Z_4 had lengths, in terms of numbers of sectors, of 1, 4, 8, 9, 12, and 17. Z_0 had some records on it with 51 sectors on them. The "small" records being used frequently correspond to commonly used system routines.

(4) Access time was mostly below 1 msec in all the three discs, with a few occurrences at 50 msec. point.

(5) Head positioning time had a more or less normal distribution.

More data will be collected upon receiving the memory modules which have been sent to the manufacturer for correcting the hardware defects. Richard Staib, Edward Phillips and I plan to do this and analyze the data before the end of this year.

(b) Study of Magnetic Tape Performance:

I completed the design as well as the drawings for the plug-in modules to be used with the SDCS in order to monitor the activities in the magnetic tape storage system. Since there are 8 tape controllers in all, to be monitored, 8 identical modules are needed for the purpose. John Gambill built one such module in September 1973. Edward Phillips and I debugged it and checked it out. Seven identical modules were built later. However, they could not be debugged and checked out until today due to unavailability of one-shot chips required. I have just learned that the needed chips have been received.

The remaining seven modules will be debugged and checked out in the first half of November. I plan to hook up the SDCS with the plug-in modules onto test-points on all tape controllers sometime in December. The data obtained will be analysed and useful information for the requirements of a Mass Storage System for the complex will be obtained.

(c) Study of Application Program Efficiency:

Software programs for monitoring application programs have certain drawbacks:

(1) The sampling rate varies from 1/2 second to 50 μsec., which is not refined enough for accurate measurements.

(2) It increases the application program run time and memory size requirements by 0 to 15%.

(3) The monitor program may interact with the application program to such an extent that the characteristics obtained by monitoring may be completely different from the real characteristics of the application program being monitored.

In view of the above drawbacks of a software monitor, a hardware monitor is the way to go about monitoring an application program. I designed plug-in modules to be used with the SDCS in order to monitor an application program. This will give us the frequency of execution of various instructions in the application program and thus show the amount of time that the computer is spending at these instructions. If an application program is caught in some loop in it, the plug-in module can be used to locate such loops in the program. This would provide very significant help towards debugging an application program. Also, if one attempts to decrease the length of a rather lengthy Fortran program by changing a few lines of code, the module can be used to determine which areas of the program should be considered for improving the efficiency of the program.

The application program to be checked will be run on a CDC 6400 computer. Arrangement will be made with system analysts and CDC customer engineer to provide a code for such a program so that when the program is being executed, a predetermined flag will be turned on. Whenever an instruction in the program to be monitored is executed the corresponding location in the memory of the data collection system will be incremented.

The data will be accumulated in one half of the memory of the Data Collection System while the other half is transferring data to the tape.

The drawings for the design are ready and the modules will be built sometime in December. Debugging and checking out of the modules will be done in early part of the year, 1974.

(d) Study of CPU Performance:

In order to study the nature of computing done at the Center in terms of frequency of use of various arithmetic units, and conflicts in their accesses, the number of instructions executed per second, etc., I designed plug-in modules for monitoring a CDC-6600 central processor unit.

The plug-in module designed for the purpose can, also, be used for determining the efficiency of different higher level languages in terms of frequency of distinct arithmetic operations that they involve for a given computing job. For example, a comparison between the efficiencies of Fortran-Run (currently in use) and Fortran-Extended (to be used in the near future) languages for a given job in terms of distribution of various arithmetic operations, can be made.

The drawings for the modules are ready. The modules will be built around the end of February and the system implemented thereafter.

(e) Simulation Model for the Computer Complex:

An effort has been underway for the last 5 months to develop a simulation model for the Computer Complex at the Center. The model can be useful in determining the effect of addition and/or deletion of subsystems in the Computer Complex, of changes in job scheduling and/or resource allocation algorithms, and of the fluctuations in the user job characteristics.

George Canovos, Joseph Drozdowski and I reviewed, from time to time, a trace-driven model that Steve Sherman of ICASE was developing during the summer. He modelled the whole complex but the refinement of the model was limited by the amount of data available from dayfile. Availability of more details regarding the events occurring in the Computer Complex would certainly help further refinement of the model. The accuracy of a model is dependent on the extent of refinement of the model.

Due to limited time at his disposal, Sherman could not complete the model. Robert Deacle of C&S has been working on the program passed onto us by Sherman. He has been debugging and flow-charting it. After the program is thoroughly checked out, it will be tested for validation of the model. Also, attempts will be made to make the model as flexible as possible in order to incorporate in it the capability of introducing changes in existing algorithms for resource allocation, changes in equipment and also changes in their characteristics.

The simulation effort is likely to go on indefinitely. It is expected that simulation will become the most outstanding computer performance evaluation tool as well as an important tool almost indispensable in the design of complex computer systems.

(f) Computer Networking:

In order to provide orderly growth, absorption of new heterogeneous systems into the complex with lease inconvenience to the users and minimal changes in operating system, manageability on a total system as well as subsystem basis, resource sharing, resource availability, installation of a Mass Storage System for the whole complex, etc., the networking of computers is necessary and under consideration at the Center.

In collaboration with Richard Hofler, Richard Staib and Donald Booth, I have been studying the advantages and disadvantages of networking of computers, different topologies as well as concepts for such networks, redundancies needed, reliability considerations, realizability in terms of the current state of technology, its impact on the expertise of the technical community here, etc.

By the end of February, I will prepare a report on my comments regarding networking of computers at the Center.

(g) Ph.D. Thesis Review:

Jerry Tucker has been working on his Ph.D. Thesis "Transitional Calculus using Boolean Differences" for the last 15 months. I have been reviewing his research progress as well as technical writing of the dissertation.

The work presents a sophisticated, mathematical way of analyzing and synthesizing sequential systems that have edge-sensitive elements in them.

The writing of the thesis is expected to be completed before the end of the year, 1974.

III. Other Activities

I developed programs for obtaining compatibility classes and maximum compatibility classes for an incompletely specified sequential system. This will help in design of such systems.

In March 1973 Richard Staib, Joseph Drozdowski and I visited the laboratory of Tesdata Systems Corporations in order to see a demonstration of their system 1185. We were quite impressed with the sampling rates as well as flexibility of the system to measure and record simultaneously a number of parameters of a computer system.

In March 1973, Richard Staib and I attended the Computer Performance Evaluation Users Group meeting held at the Naval Postgraduate School in Monterey, California.

In May 1973, I attended the IEEE Southeast-con held in Louisville, Ky. to present my paper, "State Equations for Linear Time-Varying Networks".

In June 1973, George Canovos and I attended the first-ever symposium on Simulation of Computer Systems held at the National Bureau of Standards in Gaithersberg, Maryland.

In October 1973, I attended the Eleventh Annual Allerton Conference on Circuit and System Theory held at Monticello, Illinois in order to present my paper "The Effect of Augmenting Reactive Elements in an Improper Network on its State Equations".

The reports on all the conferences mentioned above are on file in the Digital Systems Branch in the Analysis and Computation Division.

IV. Conclusion

The extent as well as the depth of my involvement in the activities in the Computer Complex has increased considerably. I have had invaluable experience in the design, debugging and installation of hardware monitor systems as well as in the development of a discrete event simulation model for the Computer Complex at the Center.

The opportunity to review deeply the Ph.D. thesis in the area of Transitional Calculus has introduced me to a new open and promising area which has the potential of making good contribution in terms of giving novel techniques for analyzing and synthesizing sequential systems.

The totality of my experience here has increased the depth and the breadth of my background in Computer Engineering.

File - E-21-622

RESIDENT FELLOWSHIP PROGRAM

IN

COMPUTER SCIENCE

SEMI-ANNUAL STATUS REPORT NO. 3
NASA GRANT NO. NGR 11-002-158

NOV. 1, 1973
TO
APRIL 15, 1974

BY

MOIEZ A. TAPIA

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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RESIDENT FELLOW PROGRAM

IN

COMPUTER SCIENCE

MOIEZ A. TAPIA

I. Review of earlier work:

My principal assignment in the Analysis and Computation Division of the Langley Research Center is the evaluation of performance of various subsystems in the Computer Complex using a Statistical Data Collection System (SDCS). Towards this end, as reported earlier (1,2) Richard Staib, Edward Phillips and I designed plug-in modules for monitoring disc storage system, debugged the system and checked it out using hardware simulation systems designed for the purpose. Also, I designed plug-in modules for monitoring tape storage system, central processing unit and application programs.

I have been reviewing Ph.D. dissertation of Jerry Tucker. I have been studying various aspects pertaining to definition of, and specifications for a local computer network that is under consideration at the Center.

Also, I have been reviewing efforts underway at the Center towards developing a simulation model for the Computer Complex.

II. Status of Specific Task Assignment:

(a) Study of Disc Performance. -

As reported in (2), the Ampex memory module in SDCS needed reapir and was sent to Ampex factory for repair in October 1973. On receiving it, Edward Phillips and I checked it out, and the SDCS connected it to test-points of disk controllers Z_0, Z_3 and Z_4 and gathered data during the period Feb. 24, 1974 through March 4, 1974. Later he and I connected the SDCS to the test-points of disk controllers B_0 and B_4, and gathered data during the period March 24, 1974 through March 30, 1974.

The data is being currently reduced. Detailed analysis will be reported in a memo to be written after all the data have been analyzed. The initial results are comparable to those obtained in September 1973.

(1) The distribution of records written (and read) in terms of their lengths indicate a need for examining the block size, for writing records, of our operating system. 70% or more of the records have lengths in the range of 1 to 7 sectors. If the block size were redefined so that such small records would not have to be normally used, the number of records read (and written) can be reduced. This would result in reduction of total time spent in accessing and repositioning, thus increasing the total time spent in reading or writing activity and improving the overall efficiency.

(2) The mean repositioning time was around 60 mseconds.

(3) The average rate of parity error occurrence was about 70 per billion bits transmitted. Since at present we have nothing to compare this value with, it is difficult to comment on it. It is interesting to observe here, however, that the rate of occurrence of parity errors in our tape storage system is of the order of one error per a million bits transmitted.

(4) The maximum number of reads and writes per second was 112, which is much below theoretical maximum of 1000.

(5) The difference in the activities in Z_0 and Z_4 was observed as before (80% and 60%), which is significant. A more efficient operating system would tend to balance the load on the two discs.

(6) Total activity on Z_3 (the job disc) was observed to be very poor as before. This indicates a very inefficient utilization of the disc. Consideration should be given to using a tape for keeping job records on it so as to be able to use the disc Z3 in a much more efficient way for other purposes.

The analysis of data obtained has given us information regarding the status of the performance of the disc storage system. The next objective would be to make changes in operating system and different algorithms associated with the disc system and analyze them in order to determine the effect of the changes made on the performance. In a dynamic environment such as exists in the complex, periodic use of the SDCS would help us not only to learn more about the system behavior but also run the system most efficiently.

(b) Study of Magnetic Tape Performance. -

Edward Phillips and I debugged and checked out the 8 identical modules designed for monitoring Tape Storage System. He and I plan to check out the SDCS with these modules in it and the probes and cables connected to receiving end of the system. The SDCS will, then, be connected to the test-points of tape controllers sometime in May and data will be gathered and analyzed. This will give us useful information for

the requirements of a Mass Storage System for the Complex.

(c) Study of Application Program Efficiency. -

The superiority of a hardware monitor over a software monitor has been discussed earlier (2). Also, the plug-in modules I designed for monitoring application programs has been described in an earlier report (2). The modules will be built and debugged in June 1974.

(d) Study of CPU Performance. -

In order to study the nature of computing done at the Center in terms of frequency of use of various arithmetic units, conflicts in their accesses, the number of instructions executed per second, etc., I designed plug-in modules for monitoring a CDC-6000 central processor unit.

The modules will be built and debugged sometime in early July and the SDCS with these modules in it will be connected to the test-points of a CPU of a CDC-6000 computer.

(e) Simulation Model for the Computer Complex. -

The need for and the philosophy of developing a simulation model for the Computer Complex have been described in an earlier report (2). George Canovos, Joseph Drozdowski and myself have been reviewing the efforts underway for developing simulation model for the Computer Complex.

Robert Deacle has been debugging the model left to us by Sherman at the end of Summer 1973. The model at present takes nearly 0.93 unit time to run jobs which took 1 unit of time under real ICOPS system. Also, to run jobs that took 24 hours under real ICOPS system, the model takes nearly 16 minutes of CPU time and 160K words of CM.

The inaccuracies in the model stem from lack of certain information available from dayfile as well as discrepancies of the model itself. The dayfile does not tell us as to when a job goes into premount and when user subroutine EVICT releases a tape. The model does not use information regarding data cell down time and WAITGO control card. Also, the model is not handling big jobs running at midnight, the way they should be handled.

The accuracy of the model will be improved in the next couple of weeks by refining the model as well as modifying the dayfile subroutines.

After "reasonable" accuracy has been obtained, the effect of changes in algorithms for assigning printers on the throughput will be determined using the model. The effect of changes in other algorithms and/or resources will be determined later.

Simulation models and hardware monitors are complementary and indispensable for understanding behavior and improving the efficiency of the computer complex.

(f) Computer Networking. -

In a sense we already have a computer network, since the five CDC-6000 computers have been integrated into a system which permits communication between any two components in the system. The present system, however, is limited in a number of ways and steps must be taken to improve the computing facility available to users in the near future.

A computer network for the Center that is being defined and is under study is needed for a number of reasons. Such a network would permit orderly growth with little of no interruption to smooth running of the computers at any time, provide an easy manageability of the whole complex and load leveling among the various components, and encourage greater cooperation and communication among different experts.

Some of the advantages of having a local computer network are:

(1) Avoidance of duplication of data.

(2) Avoidance of duplication of software.

(3) Enhancement of file security by causing all references to files to go through a standard procedure.

(4) Simplification of conversion to remote batch terminal.

(5) Avoidance of the manual transfer of file from one computer to another.

(6) The need for amassing computers from a single manufacturer is avoided, thus allowing the computer complex to be heterogeneous and hence rich. This in turn leads to reduction in problems associated with replacement, premature obsolescence, the phasing in and out of equipment and consequent disruption of operations.

(7) Problems associated with forecasting and planning of computer requirements are simplified.

(8) From a purely computing viewpoint, probably the most important benefit of a computer network is the useful rationalizing influence that they can have on computing itself. Many of today's computer related problems arise out of irrational, uncontrolled developments that have taken place in hardware, operating systems, languages, data structures, etc. These are obstacles not only to networking but also to computing efficienty per se. Networking of computers

will force users as well as different manufacturers to face the problems arising out of arbitrariness and lack of standards. The tendencies to work in isolation and staying aloof will diminish. People will see to it that it is in their advantage to conform to standards and will make conscientious efforts to do so.

(9) The reluctance to try out new systems of various companies will diminish. This will give rise to a healthy competition among manufacturers that will result in improved services to users.

Due to the "local" nature of the computer network under the consideration at the Center, the Center has certain advantages in the sense that the topological constraints on the network design are minimal. For a large nationwide or even statewide network, topological constraints would play an important role in the design of network.

The store-and-forward type of network with a central box responsible for storing and forwarding messages, as proposed by Richard Hofler (private communication) should receive serious consideration. This should, however, be compared with switched-packet network in which a fixed block of data transmitted by a system in the network moves through the network and is retransmitted by various systems in the network when it is not meant for them and thus finally reaches where it is intended.

The data transfer rate should be kept as high as current technology can allow. (Current Bell Telephone Systems rates are of the order of 6.6 Mb/s). Since the future computers, memory systems and other peripherals are going to have much faster speeds than the present ones, full advantage of these high speed can be taken only if the data transfer rate per channel is kept highest possible to start with.

Necessity of providing redundance in the central switching unit should be considered. If there is a breakdown in this unit, the total intercommunication comes to a halt.

Also, redundance of channels between the central unit and various other units should be studied from cost and reliability point of view. In particular, the reliability of the link between mass storage unit and the central unit should be given due weight while designing the system.

Some desirable features of protocol languages:

(1) Operations the user performs very often should be expressed by a single command. This will minimize programming errors and it will allow for optimization of command control.

(2) As new operations are required, they should be able to be added to the language without affecting already defined commands.

(3) Purely system requirements should be invisible to the user.

(4) The language should be easily adaptable to changes in network configurations.

(5) The language should provide easy access to all features of the network at a number of degrees of sophistication.

(6) The language should provide a method for obtaining on-line documentation about the available resources.

(7) Options used to determine which computer system you are communicating with should not have to exist in interpretable code. If it does, data conversion can only be performed at low speed.

A hardware monitor device may be placed at one of the ends of every channel in order to determine the data flow rates and the total amount of data flow during a given interval.

The area of network performance measurement has barely been touched upon. Continued development and testing of internal measurement techniques is needed along with substantial attention to measurement criteria, specific measures and measurement tools for externally determining the performance of all types of computer networks.

It is too early to conclude which way we should be going as far as computer networking is concerned. It appears that finalization of the type of Mass Storage System we are going to have should precede our finalization of computer network that we will have.

(g) Ph.D. Thesis Review. -

I have been reviewing research of Jerry Tucker. He has concluded his research in the area of transional calculus using Boolean differences, as far as his Ph.D. thesis is concerned.

He has established conditions for integrating Boolean differentials and obtained algorithms for integrating compatible differentials and exact differentials. He has given an algorithm for piecewise-integrating any differential.

The results are a significant contribution to the design of sequential systems using edge-sensitive flip-flops and to fault analysis. Much work remains to be done in this area and it has a good potential for many applications.

The writing of the Ph.D. thesis is in progress and is expected to be finished some time in May 1974.

III. Other Activities:

I wrote a NASA Techbrief (in press) described in Appendix I. It gives a quick way of finding distribution of current into various branches of a large series-parallel network, when the element values are described in terms of their admittances. If the element values are variables, then one can express them in terms of their admittances and find the distribution of the current

entering the network into its various branches.

The Techbrief is expected to be published by September 1974.

I, with important contribution from Jerry Tucker, established necessary and sufficient condition for solution of a system of Boolean equations with k unknown functions of specified number of variables.

This is a significant contribution. The early approaches used matrix transformations and involved some trial and error to solve the system of equations. The method obtained shows how to find solutions readily without any trial and error or matrix transformations. Also, it points out the exact number of solutions that exist for a given system of equations.

I presented the results at the Sixth Annual Southeastern Symposium on System Theory, Baton Rouge, Louisiana, Feb. 21-22, 1974.

A copy of the paper presented is given in Appendix II.

Design of modules for monitoring various aspects of operating system in the complex is currently under study. This is, indeed, a very significant and useful activity which may not be completed before the end of the current grant extension.

IV. Conclusion:

The design of the modules for monitoring disc storage system has been successfully completed. The SDCS is now operational for monitoring disc system and will be used periodically.

The analysis of the initial data obtained has already given us insight into the status of performance of disc system and has indicated possible ways of improving performance.

The design of modules for monitoring tape storage system, application program and central processor unit is close to completion.

Important aspects of a local computer network have been outlined. Not much, however, can be done towards this and until the plans for a Mass Storage System are finalized.

The Ph.D. Thesis in progress is close to completion.

The necessary and sufficient conditions for existence of solution of a system of Boolean equations have been established and a simple algorithm for obtaining the solutions has been obtained.

As far as my personal experience is concerned it has varied from highly experimental, down-to-nuts-and-bolts hardware level to highly abstract theoretical level. The wide spectrum of experience coupled with the relevance and the practicality of the activities pursued have gone a long way towards realizing the goals of ASEE Resident Fellowship.

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Appendix I

Generalized Current

Distribution Rule

GENERALIZED CURRENT DISTRIBUTION RULE

The method presented in this Tech brief helps one to determine, by instpection, the branch current in a parallel-series network in relation to the total input current. It is particularly useful for circuits with many elements, when the branch elements are described as admittances. If the element values are variables, then one could express these values as admittances and readily find currents in desired branches.

INTRODUCTION

A parallel-series network, N, with k branches b_i, $1 \geq i \geq k$, in parallel, with branch b_i comprising admittances $g_{i,1}$, $g_{i,2}$, ..., $g_{i,ni}$ in series, has current I entering at its terminal node 1 and leaving at its terminal node 1' as shown in Figure 1. It is intended to obtain an expression for the current ratio I_i/I, where I_i is the current in the branch b_i.

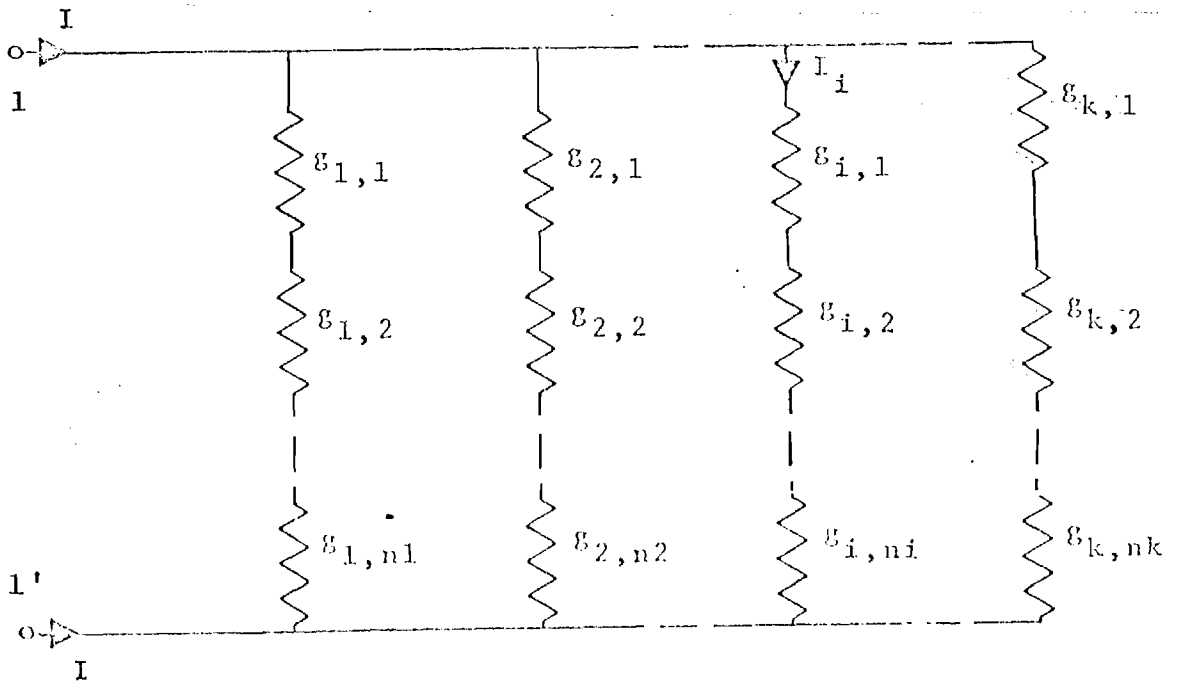

Figure 1

Let P_i = product of all admittances in ith branch

$$= \prod_{j=1}^{n_i} g_{I,j}$$

Q_i = sum of products of admittances in the ith branch taken (ni-1) at a time, if (ni-1)>0

Q_i = 1, if ni = 1.

Q = sum of 2-tree admittance products of the network

$$= \prod_{i=1}^{k} Q_j$$

T_i = sum of admittance products of all those trees that intersect in the branch b_i

= ith tree admittance products sum

$$= P_i \; Q \; Q_i^{-1}$$

$$T = \sum_{i=1}^{k} T_i = \text{sum of tree admittance products of N.}$$

I_i/I

$$= \frac{\text{(admittance of branch } b_i)}{\text{(admittance of total network)}}$$

$$= \frac{\text{sum of tree admittance products of branch } b_i.}{\text{sum of 2-tree adm. products of } b_i} \cdot \frac{\text{sum of 2-tree adm. products of N}}{\text{sum of tree adm. products of N}}$$

$$= P_i/Q_i \; . \; Q/T$$

$$= (P_i Q . Q_i^{-1})/T$$

$$= (T_i/T) \qquad (1)$$

$$= \frac{\text{ith tree admittance products sum}}{\text{(sum of all tree admittance products of N)}}$$

Equation (1) gives the generalized current distribution rule in terms of topological concepts, which can be easily

obtained by inspection. Familiarity with topological concepts is, however, not necessary in order to find the right hand side of equation (1) in terms of $g_{i,j}$,s. T_i can be looked upon as a product of k terms, each corresponding to a branch of N, with ith term consisting of product of all admittances in the ith branch and the jth term, $\forall j \neq i$, consisting of sum of products of all possible (nj-1) admittances in the jth branch, the jth term being unity if and only if nj = 1.

Example: Consider the network in Figure 2.

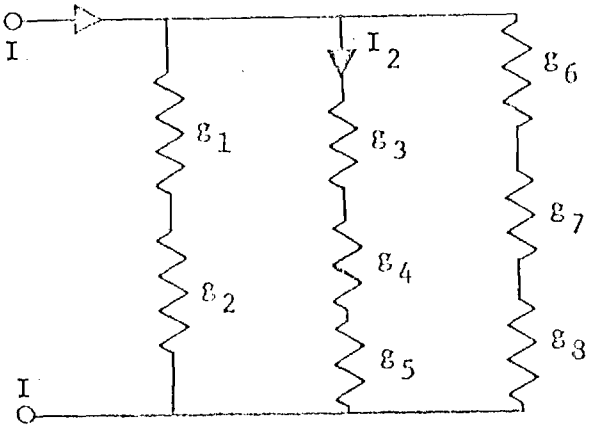

Figure 2

$$I_2/I = (g_1+g_2)(g_3g_4g_5)(g_6g_7+g_6g_8+g_7g_8)\cdot$$
$$[(g_1g_2)(g_3g_4+g_3g_5+g_4g_5)(g_6g_7+g_6g_8+g_7g_8)$$
$$+ (g_1+g_2)(g_3g_4g_5)(g_6g_7+g_6g_8+g_7g_8)$$
$$+ (g_1+g_2)(g_4g_5+g_4g_3+g_5g_3)(g_6g_7g_8)]^{-1}$$

CONCLUSION

It has been shown that in a parallel-series network, the fraction of current flowing into the network, that flows into a branch of the network is proportional to the sum of admittance products of those trees of the network that include the branch.

Note:

Requests for further information may be directed to:

Technology Utilization Officer

Mail Stop 139-A

Langley Research Center

Hampton, Virginia 23665

Patent status:

No patent action is contemplated by NASA.

Source: Moiez A. Tapia

ASEE-Ford Foundation Resident Fellow

Langley Research Center

(LAR-11565)

Appendix II

Solution of Boolean Equations

and

Their Applications

SOLUTION OF BOOLEAN EQUATIONS AND THEIR APPLICATIONS

Moiez A. Tapia

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ORGANIZATION

ABSTRACT

Necessary and sufficient conditions for the existence of one or more solutions for a system of Boolean equations are given and an algorithm for obtaining these solutions is outlined. If a solution does not exist for a given system of equations, then the constraints under which the system can be solved, are, also, given.

INTRODUCTION

The solution of a set of Boolean equations of the form given in set of equations (1) has been studied earlier [1,2,3,4]. We will consider k simultaneous Boolean equations of the form given below

$$\begin{aligned} f_1 &= h_1 \\ &\vdots \\ f_k &= h_k \end{aligned} \qquad (1)$$

where f_i and h_i, for all i are Boolean functions of m unknown Boolean functions g_1, g_2, ---, g_m and n independent variables X1,X2,---,Xn. g_i, for all i, is also a function of X1, X2, ---, Xn.

It can be shown that the system of equations in (1) is equivalent to equation (2) given below.

$$(\bar{f}_1 h_1 + f_1 \bar{h}_1) + (\bar{f}_2 h_2 + f_2 \bar{h}_2) + \cdots + (\bar{f}_k h_k + f_k \bar{h}_k) = 0$$

The equation (2) will be called the characteristic equation of the Boolean system defined by equation set (1). The equation (2) will be expanded as a sum

$$F_0 G(0) + F_1 G(1) + \cdots + F_{2^m-1} G(2^m-1) + K \qquad (3)$$

where G(k) is the minterm of variables $g_1, g_2, \ldots, g_m$ k being the value of binary number obtained by replacing g_i's and their complements by 1 and 0, respectively, and F_i is the sum of some of the minterms X(0), X(1),---, $X(2^n-1)$, or a constant (0 or 1). The function K is a function of X1, X2, ---, Xn, and not a function of g_i's. It is assumed that equation (2) is obtained to that there is no minterm of X_i's common to F_0, F_1, ---, F_{2^m-1}. The characteristic equation, will, then, be said to be in standard form. The coefficient matrix, H, of the system (1) is defined as a $2^m \times 2^n$ matrix such that

(1) the rows correspond to G(i)'s,
(2) the columns correspond to X(j)'s
(3) the entries are "blanks" or zeros
(4) $h_{ij} = 0$ if F_i includes minterm X(j) in it. h_{ij} is left blank otherwise.

It is obvious from equation (3) that if $K \neq 0$, the system of equations in (1) is not solvable. Thus $K = 0$ is the necessary condition for existence of a solution of the system. It will be shown, next, that this condition is also sufficient for the existence of a solution.

Assume $K = 0$ and consider the column j corresponding to the minterm X(j), $0 \leq j \leq (2^n-1)$. Since no minterm of X_i's belongs to F_p, for all p, there is at least one entry say i^{th} entry in the column which is blank. We will make G(i) = 1. If g_a appears in its true (or complemented) form in G(i), we will set $g_a = 1$ (or 0). If $g_a = 1$ (or 0), the minterm X(j) will be included (or not included) in g_a when the function g_a is constructed. By applying the same procedure to each column, the need for including or excluding the minterm of X_i's in the functions g_1, g_2, ---, g_m will be determined.

Consider the j^{th} term $F_j G(j)$ in equation (3). In virtue of the way we have constructed the function g_i's, none of the minterms of X_i's could exist in all of the functions g_1, ---, g_m. Hence the j^{th} term $F_j G(j) \equiv 0$, for all j and equation (3) is satisfied by the set of g_i's we have constructed. Hence

Theorem 1: The necessary and sufficient condition for the existence of a solution of system of Boolean equations is that the term K in its characteristic equation in its standard form, be identically zero.

Theorem 2: A solvable system of Boolean equations has a unique solution if and only if every column in its coefficient matrix has exactly $(2^m - 1)$ zero entries.

Corollary: A solvable system of Boolean equations has a unique solution, if and only if the coefficient F_i's in its characteristic equation are such that $F_i \cdot F_j = 0$ for all i,j, $i \neq j$.

Theorem 3: If $K \neq 0$ and $K \neq 1$ in the characteristic equation, in its standard form, of a system of Boolean equations, then $K = 0$ is the constraint that must be imposed on the system in order to be able to solve the system.

ALGORITHM

1. Obtain the characteristic equation, in standard form, for the given set of equations. If $K \neq 0$, no solution exists. If $K = 0$, go to next step.
2. Under every column corresponding to a minterm in F_0, place a zero in 0^{th} row. Repeat this for minterms in all other coefficients F_1, F_2, --- and placing zero in 1st, 2nd -- rows respectively. The coefficient matrix has now been constructed.

3. Consider the 0^{th} column. Assign all possible sets of values (0, 1 or X) to $g_1, g_2, \cdots, g_{2^m-1}$ so that for each set of values the value of the minterm G(k), for any k, is zero, whenever the corresponding (k^{th}) row has zero under this column. 0(or1) value assigned to g_i, for i, signifies that the minterm X(0) should not be (or should be) included in g_2.

4. Repeat step #3 for the remaining columns. All possible sets of functions $g_1, g_2, \cdots, g_{2^m-1}$ (obtained) are the solutions of the system.

EXAMPLE

Consider a system of boolean equations whose characteristic equation in the standard form is

$$(X(0)+ X(3) + X(7))G(0) + (X(2) + X(3))G(1) + (X(0) + X(2) + X(3))\, G(3)=0 \qquad (4)$$

$$H = \begin{array}{c} G \backslash X \\ 0 \\ 1 \\ 3 \\ 2 \end{array} \begin{array}{c} \begin{array}{cccccccc} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \end{array} \\ \begin{bmatrix} 0 & & & 0 & & & & 0 \\ & & 0 & 0 & & & & \\ 0 & & 0 & 0 & & & & \end{bmatrix} \end{array}$$

$$\begin{array}{c} \\ g_1 \\ g_2 \end{array} \begin{array}{c} \begin{array}{cccccccc} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \end{array} \\ \begin{bmatrix} g & x & x & 1 & x & x & x & 1 \\ \bar{g} & x & 0 & 0 & x & x & x & x \end{bmatrix} \end{array} \quad g = 0 \text{ or } 1$$

$$\begin{array}{c} g_1 \\ g_2 \end{array} \begin{bmatrix} g & x & x & 1 & x & x & x & x \\ \bar{g} & x & 0 & 0 & x & x & x & 1 \end{bmatrix}$$

The last two matrices define the sets of g_1 and g_2 that are the desired solutions. Observe that these are $3 \times 2 \times 2^9 = 3072$ distinct solutions.

APPLICATION

Application of solution of a system of boolean equations in decomposition of functions (2), in formulation of cascade design (2) and in contrained-input problem (5) has already been considered. The method presented here can be useful in the solution of Boolean differential equations (6), also.

ACKNOWLEDGEMENT

The author is pleased to gratefully acknowledge various suggestions of Jerry H. Tucker, NASA Langley Research Center, Hampton, Virginia, in preparation of this paper.

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RESIDENT FELLOWSHIP PROGRAM

IN

COMPUTER SCIENCE

FINAL REPORT
NASA GRANT NO. NGR 11-002-158

JUNE 12, 1972
TO
SEPTEMBER 12, 1974

BY

MOIEZ A. TAPIA

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
LANGLEY RESEARCH CENTER
HAMPTON, VIRGINIA

ATTENTION:

MR. RICHARD MORRIS, NASA TECHNICAL MONITOR AND PRECEPTOR
MR. WILLIAM F. GIANNINI, GRANT ADMINISTRATOR

School of Electrical Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332

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RESIDENT FELLOW PROGRAM

IN

COMPUTER SCIENCE

MOIEZ A. TAPIA

I. General Assignment

My principal assignment in the Analysis and Computation Division of the Langley Research Center was the evaluation of the performance of various subsystems in the Computer Complex using Statistical Data Collection System (SDCS). The system uses a large number of high-speed probes, integrated-circuit logic and storage media for capturing and storing desired events.

In collaboration with Richard Staib and Edward Phillips I designed systems for monitoring disc controller, tape controller, program count register and central processor unit for studying the performance of disc storage system, tape storage system, central processor unit and efficiency of application programs respectively. These systems are described in earlier reports (1, 2, 5).

Among other activities, I intensively reviewed and consulted in the preparation of a Ph.D. thesis by Jerry Tucker, who received his Ph.D. degree in June 1974. I reviewed efforts, in the Center, to develop a Simulation Model for the Computer Complex. I was, also, involved in the study of a Computer Network for the Complex. All these activities will be described in the next section.

II. Specific Assignments

(a) Study of Disc Performance

The purposes of studying disc performance as well as the details of the plug-in modules for monitoring the disc controller have been described in earlier reports (1, 2, 5).

The Statistical Data Collection System was connected to discs Z_0, Z_3, and Z_4 and data collected during the week Feb. 25, 1974 through March 2, 1974. Later it was connected to discs B_0 and B_4 and data collected during the week March 25, 1974 through March 30, 1974.

The statistical analysis of various parameters measured is given below:

(1) The total activity time is the time spent in accessing, repositioning, reading and writing. Useful activity time is the time spent in reading and writing records. The average total activity on Z_0, Z_3, Z_4, B_0 and B_4 was found to be 35.6, 2.3, 13.0, 40.7, and 28.8% respectively.

(2) The percentage of records written with length less than or equal to seven sectors is around 80% in all the discs.

In case of Z_3 more than 80% of the records written were of one-sector length. This indicates a poor definition of currently used block size. Consideration should be given to redefining block size so that most of the records written would be of 8-sector length. This would reduce time spent in accessing and/or repositioning thus improving overall data transfer rate.

The percentage of records read, with length of seven or less sectors was in the range of 60 to 80.

(3) The maximum number of sectors read and written in a fifteen-minute interval was 191,854 (B_0) and 66,198 (Z_4) respectively.

(4) The mean repositioning times for Z_0, Z_4, B_0 and B_4 were 51.55, 58.37, 35.45, 42.50 and 39.20 milliseconds respectively. The repositioning time had nearly uniform distribution over the range 17-92 millisec. For Z_3 the range was 62-91 millisec.

(5) 90% of accesses took less than 2 milliseconds. Some accesses took 50 milliseconds.

(6) The number of parity errors per billion bits transmitted was 64, 867 and 81 for Z_0, Z_3, and Z_4 respectively.

The percentage of time spent in useful activity, on the average, was found to be 3.42, 0.14, 2.57, 5.06 and 3.93 for Z_0, Z_3, Z_4, B_0 and B_4 respectively.

This indicates a very low activity on job disc Z_3 and hence a very inefficient utilization of the job disc. Consideration should be given to writing job copies on a tape or another disc.

Significant unbalance exists between activities on Z_0 and Z_4, and some unbalance between B_0 and B_4.

The maximum total activity during a 15-minute interval was found to be 85.9, 9.7, 61.0, 93.6, and 92.2 on discs Z_0, Z_3, Z_4, B_0 and B_4 respectively.

(b) Study of Magnetic Tape Performance

The study of performance of the magnetic tape storage system was undertaken in order to obtain information needed for determining the requirements and specifications for a Mass Storage System for the Complex. The plug-in modules designed for the purpose have been described in an earlier report (1). Ed Phillips and I debugged and checked out the system with the help of John Gambill. The SDCS was connected to the tape controller for nearly 6 consecutive days during July 1974. Partial analysis of the data gathered has been recently obtained. The following statistics are based on analysis of data gathered from 8:20 a.m. to 8:20 p.m. on Monday August 5, 1974.

Mean Record Length = 236 CM words

Records Written (during the twelve hour period) = 90,923

Records Read = 286,580

Records Read or Written = 370,449

Back Spaces = 4729

Parity Errors = 8621

Files = 347

Records/File = 1068

Mean File Size = 251,906 CM words

Tape Mounts - 346

Rewind/Unloads = 356

Maximum Transports Active During 30-second Interval = 9

Rewinds = 545

These results were compared with the information on dayfile. It was observed that as far as the monitored tapes, other than the calcomp ones are concerned, there is close agreement between the data gathered by the SDCS and those on the dayfile. Ed Phillips has looked into this problem recently. The calcomp tapes at the end of a file backspaces. This is not recorded on the dayfile, but is observed by the SDCS and recorded.

Ms. Barbara Polak has been processing the data gathered on tapes DEP 10 through DEP 14. Detailed analysis will, then, be obtained.

(c) Study of Application Program Efficiency

The superiority of a hardware monitor over a software monitor has been discussed earlier (2). A hardware system monitoring an application program can be used for debugging the program. Since it gives the distribution of frequency of execution of various instructions, it can be used to compare a pair of high-level languages, in terms of various arithmetic and logical operations they involve for a given computational job.

The details of the plug-in modules I designed are given in earlier reports (1, 2, 5). Ed Phillips and I debugged and checked out the modules wired by John Gambill. The SDCS with the plug-in modules in it, was connected to the Computer A in August 1974, and a test program written by Joseph Drozdowski was monitored. The analysis of data gathered has been obtained recently (September 1974). The system did record the frequency of various instructions executed. However, the system erroneously recorded a very frequent reference to the address 0. This fault, probably, is due to the inappropriate delay in the system between occurrence of the program clear pulse and the loading of the data from P register into the shift register in the system. Ed Phillips is considering this possibility and attempting to remove the fault.

(d) Study of CPU Performance

In order to study the nature of computing done at the Center in terms of frequency of use of various arithmetic units, conflicts in their accesses, number of instructions executed per second, etc. I designed plug-in modules for monitoring a CDC-6000 central processor unit.

The plug-in modules designed for the purpose can be used for determining efficiency of different higher level languages in terms of frequency of distinct arithmetic operations that they involve for a given computing job. For example, a comparison between the efficiencies of Fortran-Run (currently in use at the Center) and Fortran-Extended (to be used in the near future) languages for a given job in terms of distribution of various arithmetic operations, can be made.

The modules will be built in the near future and the SDCS with these plug-in modules in it will be connected to a CDC-6000 central processor unit.

(e) Simulation Model for the Computer Complex

The need for and the philosophy of developing a simulation model for the Computer Complex have been described in an earlier report (2). George Canovos, Joseph Drozdowski and I have been reviewing the efforts underway for developing simulation model for the Computer Complex.

Robert Deacle has been debugging the model left to us by Sherman at the end of Summer 1973. The model at present takes nearly 0.93 unit time to run jobs which took 1 unit of time under real ICOPS system. Also, to run jobs that took 24 hours under real ICOPS system, the model takes nearly 16 minutes of CPU time and 160K words of CM.

The inaccuracies in the model stem from lack of certain information available from dayfile as well as discrepancies of the model itself. The dayfile does not tell us when a job goes into premount and when user subroutine EVICT releases a tape. The model does not use information regarding data cell down time and WAITGO control card. Also, the model is not handling big jobs running at midnight, the way they should be handled.

The accuracy of the model will be improved in the next couple of weeks by refining the model as well as modifying the dayfile subroutines.

After "reasonable" accuracy has been obtained, the effect of changes in algorithms for assigning printers on the throughput will be determined using the model. The effect of changes in other algorithms and/or resources will be determined later.

Simulation models and hardware monitors are complementary and indispensable for understanding behavior and improving the efficiency of the computer complex.

(f) Computer Networking

Networking of the computers at the Center has been underway for quite some time. The advantages of a computer network, "local" or nationwide, have been outlined in an earlier report (5) which, also, discusses different configurations and/or protocols for a such network.

A special study group comprising Donald Booth, Richard Hofler, et.al. examined several configurations for computer networking during the summer of 1974.

Due to more intensive involvement, on my part, in tape monitoring and development of an application program efficiency monitor, I could not exchange views on the various approaches the group was considering.

(g) Ph.D. Thesis Review

I intensively reviewed and guided Ph.D. dissertation research as well as writing of the dissertation of Jerry Tucker, in the area of Transitional Calculus using Boolean Differences.

He established conditions for integrating Boolean differentials and obtained algorithms for integrating compatible differentials and exact differentials. He gave an algorithm for piecewise-integrating any differential.

The results are a significant contribution to the design of sequential systems using edge-sensitive flip-flops and to fault analysis.

He successfully defended his thesis and received the Ph.D. degree in June 1974.

III. Other Activities

Numerous professional activities such as presenting papers, publishing papers, attending seminars and conferences have been described in earlier reports (1, 2, 5). The activities not described earlier will be described here.

The research pertaining to necessary and sufficient conditions for the solution of a system of Boolean equations having unknown functions of a specified number of variables is proposed to be reported in a NASA Technical Note to be written by Jerry Tucker and I. The proposed Note will be submitted for consideration in the near future.

I attended a five-day Seminar on "Computer Performance Evaluation" held at the College of William and Mary in July 1974.

I spent several days looking into the various parameters of operating systems of a CDC-6000 computer, that could be monitored and analysed for performance evaluation and improvement. This is, indeed, a very useful and significant activity which could not be pursued to completion due to limitations on time.

IV. Conclusion

The design of plug-in modules for monitoring disc storage system and those for monitoring tape storage system has been successfully completed. Its application has given useful data whose analysis has given us insight into the status of performance of these storage systems and has indicated ways of improving the performance of the systems.

The design of modules for monitoring application program efficiency is almost completed, with some minor faults in the systems to be taken care of.

The drawings for the design of modules for monitoring central processor unit of a CDC-6000 computer have been completed.

Important aspects of a local computer network have been outlined.

The Ph.D. research was successfully completed which led to graduation of Jerry Tucker in June 1974.

The necessary and sufficient conditions for the existence of solution of a system of Boolean equations have been established, and a simple algorithm for obtaining the solutions has been obtained.

Publications accomplished include a paper in IEEE Transactions on Circuit and System Theory, a review of Wai-Kai Cheu's paper on characterization of complete directed trees and two-trees, another review of text-book "Applied Graph Theory" by Marshall, three papers presented at different conferences and a NASA Techbrief (5).

Research on solutions of Boolean equations will be submitted in a Technical Note for consideration in the near future.

The opportunity to study the hardware as well as the software systems in the Computer Complex, the experience in sophisticated design of systems to monitor some of the computer subsystems and their interfaces using modern digital design techniques, interaction with a number of experienced engineers and computer scientists, involvement in theoretical research related to digital system design - all this has tremendously contributed towards making my Residency a very worthwhile and rewarding experience for me. The extent to which this will affect the relevance and practicality of my teaching and research is immeasureable.

V. Suggestions for Extension of Work

In a dynamic environment such as exists at the Center computer performance evaluation would have to be an ever-continuing activity. It is conceiveable that additions to the complex and/or changes in the equipment or configurations will take place off and on. The effect of these changes on the performance of the computer systems will have to be determined by using hardware and/or software monitors and/or simulation models.

The plug-in modules designed for disc and tape storage systems may be used to observe the effect on performance, of any changes in different resource-allocation routines and/or various algorithms controlling processes in systems. In fact, a "best" algorithm (e.g. track assignment algorithm) for a given operation in these systems can be arrived at by varying these algorithms and observing their effects on the performance.

The plug-in modules for tape storage can be modified so that the SDCS will not record "EOF" when the tape is backspacing or rewinding.

The performance of an operating system has a tremendous effect on the overall performance of the computer using it. Consideration should be given to designing modules which can monitor various parameters of the operating system of the complex, and to determine their effect on the performance of the overall system.

Transitional Calculus as proposed by Jerry Tucker has a very good potential to make significant contribution to analysis as well as design of digital systems. It is, however, in its infantile stage. Work in this area should be continued. Necessary and sufficient conditions for a differential expression to possess an exact integral need to be obtained.

The Transition Calculus as reported in (6) assumes one variable change at a time. It should be generalized to allow multiple simultaneous changes in variables. Techniques for handling incompletely specified circuits should be developed.

Possibility of extending the applicability of Transition Calculus to circuits with input constraints should be investigated.

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